ASTRO

Interface Conversion Adaptor (DVI to LVDS)

IA-573-A

User's Manual

Ver.1.02

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(DVI to LVDS)

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2007.2

Ver.1.02

ASTRODESIGN,Inc

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Before Use

Introduction

Thank you for purchasing this DVI-to-LVDS conversion adapter (hereafter IA-573-A).
This manual contains details on the operation procedures to be followed when the IA-573-A is used, the checkpoints and precautions to be observed, and so on.
Before using the IA-573-A, please read through these instructions.
After reading the manual, keep it in a safe place for future reference.

Safety precautions

Improper handling may lead to malfunctioning or accidents. Before using this adapter, be absolutely sure to read through the safety precautions listed below: they will help to ensure that you will operate the adapter correctly.

■ **Observe the following precautions to ensure safe operation.**

⚠ **WARNING**	Do not spill liquids inside the adapter or drop inflammable objects or metal parts into it. Operating the adapter under these conditions may cause a fire, electric shocks and/or malfunctioning.	⊘
⚠ **CAUTION**	Install the adapter in a stable location. Do not stand it on its side. Rises in temperature caused by heat generation may result in malfunctioning.	❗
	Do not subject the adapter to impact. Doing so may result in malfunctioning. Take sufficient care when moving the adapter.	⊘
	When accuracy is a priority, leave the adapter for about 10 to 15 minutes after turning on its power, and wait until its operation has stabilized before starting to use it.	❗
	In the unlikely event that trouble has occurred, disconnect the adapter's cables, and contact your dealer or an Astrodesign sales representative.	❗

Packing details

The following items are included with this product.

- **Standard items**
  - IA-573-A
  - IA-573-A instruction manual (what you are reading): 1 copy

- **Optional items**
  - AC adapter, SSA0515A9
  - The IA-573-A is designed to run using this AC adapter.

AC adapter specifications

S-8453 specifications	
Rated output voltage (V)	5
Rated output current (A)	2
Input voltage (VAC)	100 to 240 (rating: 100)
Input power line frequency (Hz)	47 to 63 (rating: 50/60)

AC adapter plug shape

Plug shape	
EIAJ	RC-5320A
Voltage classification	2
Outside diameter D1	4.0
Inside diameter D2	1.7
Length (L)	9.5
Polarity display symbol	

Plug shape

1 Concerning the IA-573-A

1.1. Outline

The IA-573-A converts DVI-D inputs into LVDS and outputs them.

1.2. Features

■ **Dot clock frequency in wide band**

Table 1-2-1 shows the frequency specifications of the input and output dot clocks.

Table 1-2-1 Frequency specifications

	Operation mode	DVI input (MHz)	LVDS output (MHz)
8bit	SINGLE LINK	25 to 135MHz	
10bit	Interleave mode ON	12.5 to 82.5 (Transmission rate: 25 to 135MHz)	
	Interleave mode OFF	25 to 135MHz	

* DVI cable: When a 2-meter cable made by Molex is used

1.3. Parts and their functions

1.3.1. IA-573-A front panel

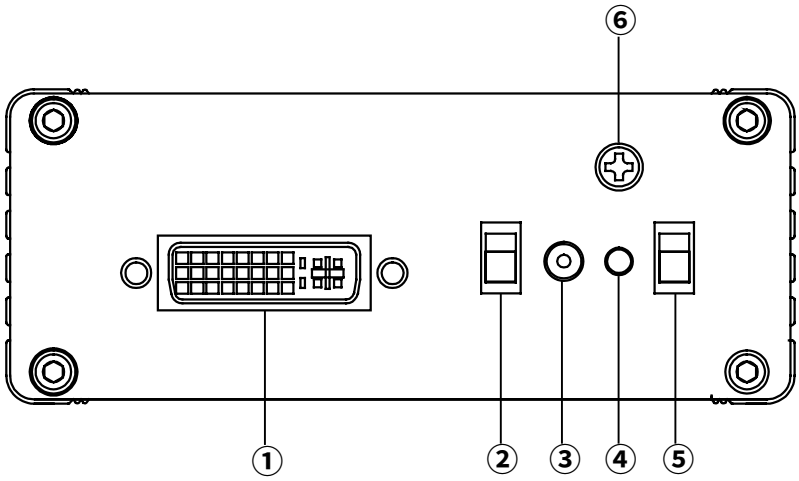


Fig. 1-3-1 Front panel

1 Input connector (DVI connector, Manner of transmission: TMDS)
2 Interleave mode selector switch: For selecting the interleave mode from ON and OFF
3 DC jack
4 LED: Lights when the power is on.
5 Power switch
6 Frame ground (FG): Connect here to share the frame ground of the equipment which is connected to the IA-573-A.

CAUTION

Always use the power switch to turn the power ON or OFF. Turning the power ON or OFF by connecting or disconnecting the cable may damage the adapter.

1.3.2. IA-573-A rear panel

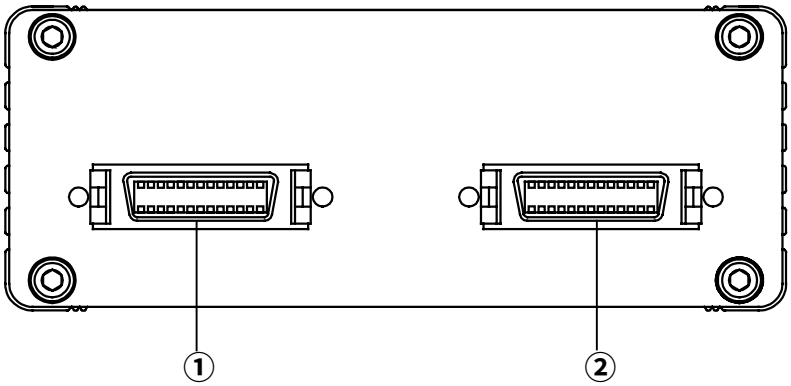


Fig. 1-3-2 Rear panel

1 Output connector 1 (DFP connector, Manner of transmission: LVDS)
2 Output connector 2 (DFP connector, Manner of transmission: LVDS)

2 Appendix

2.1. Manner of data transmission

The data will be transmitted using the interleave mode ON/OFF.

2.1.1. 12bit Dual Link transmission system

For the 12bit Dual Link transmission system, 5 TMDS lines (for data) and 1 CLK line, a total of 6 differential signals will be used. The interleave mode switch should be set OFF during the data transmission. The Figure 2-1-1 shows the 12bit Dual Link transmission system at resolution 1024 x 768, dot clock 75MHz.

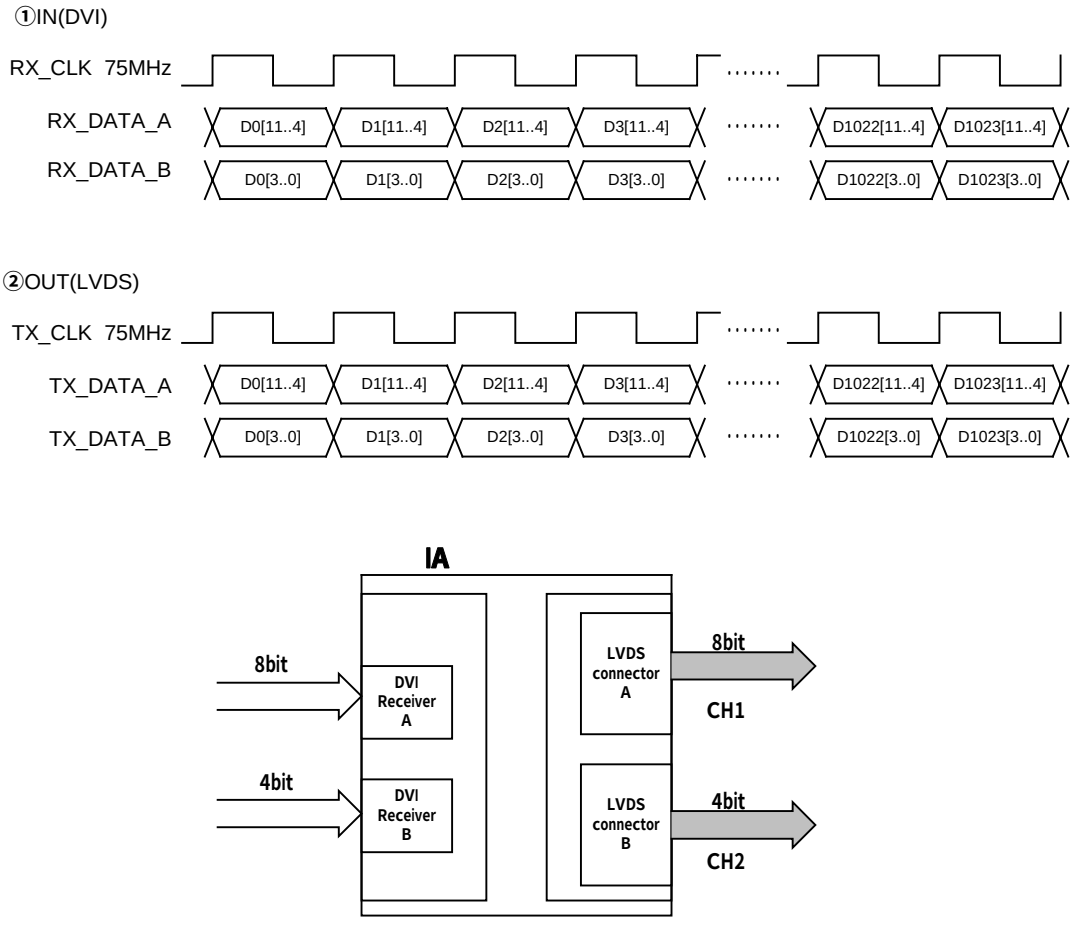


Fig. 2-1-1 12bit Dual Link data transmission system

2.1.2. 12bit Single Link transmission system

For the 12bit Single Link transmission system, 2 TMDS lines (for data) and 1 CLK line, a total of 3 differential signals will be used. The interleave mode switch should be set ON during the data transmission. The Figure 2-1-2 shows the 12bit Single Link transmission system at resolution 1024 x 768, dot clock 75MHz.

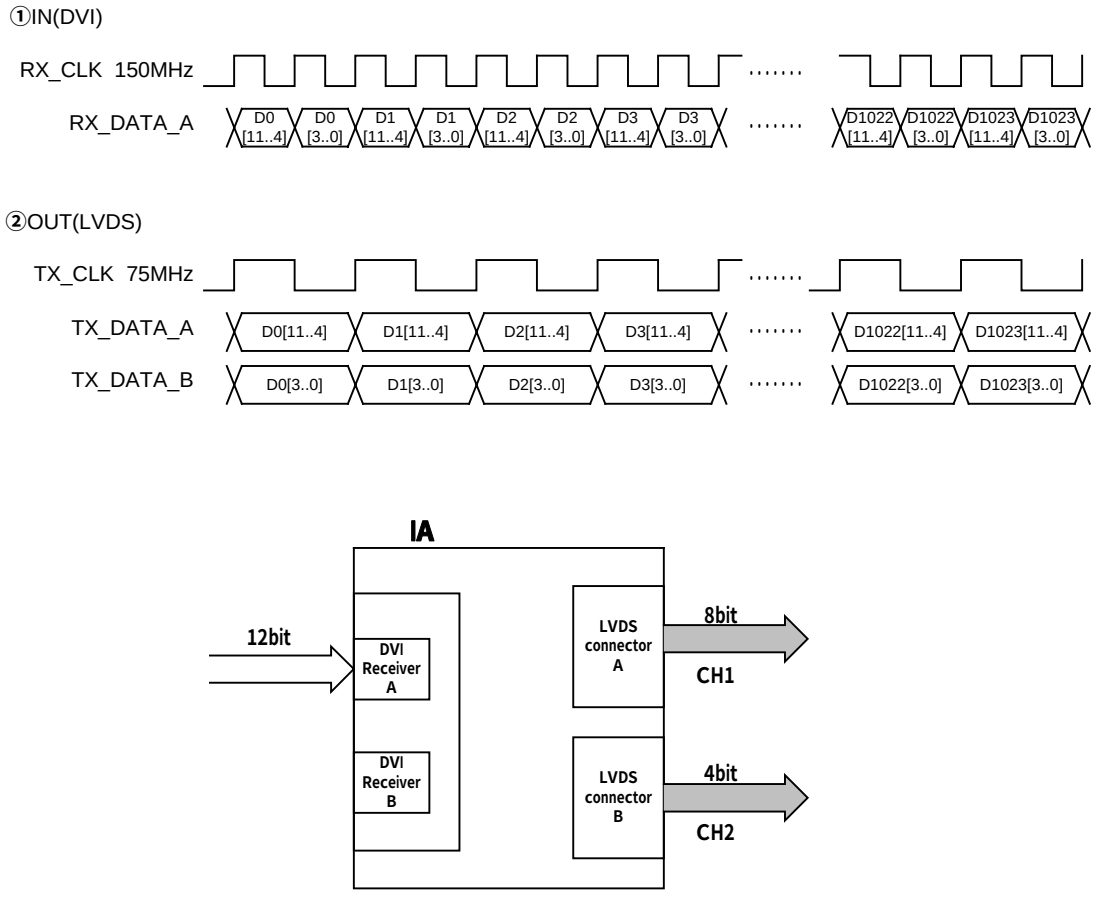
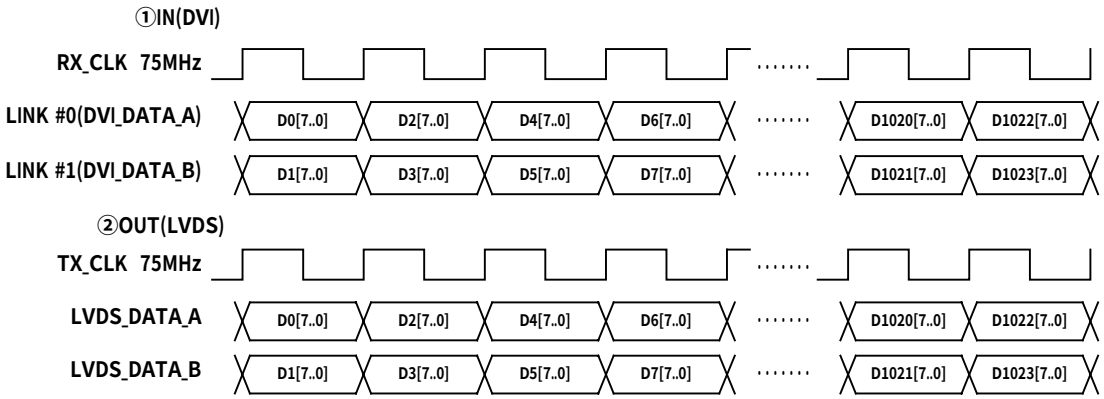


Fig. 2-1-2 12bit Single Link data transmission system

2.1.3. 8bit Dual Link transmission system

For the 8bit Dual Link transmission system, 5 TMDS lines (for data) and 1 CLK line, a total of 6 differential signals will be used. The interleave mode switch should be set OFF during the data transmission. The Figure 2-1-3 shows the 8bit Dual Link transmission system at resolution 1024 x 768, dot clock 75MHz.



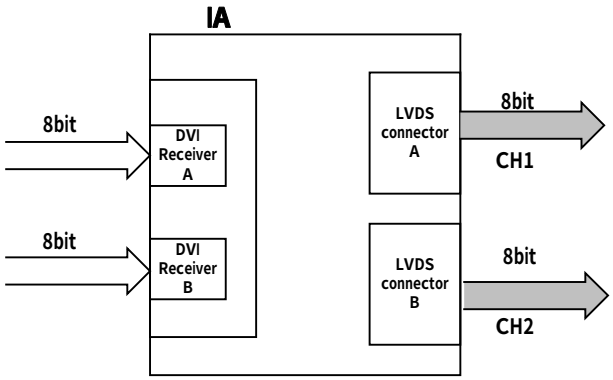
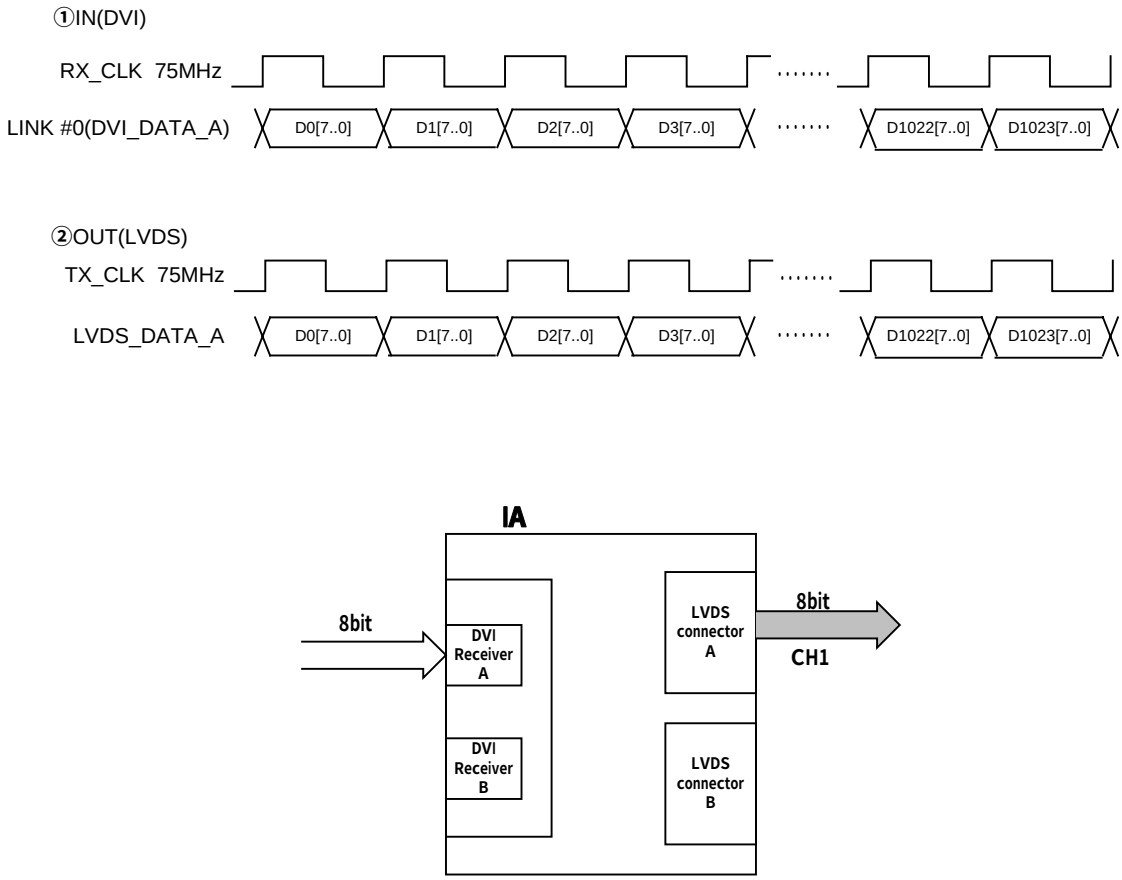


Fig. 2-1-3 8bit Dual Link data transmission system

2.1.4. 8bit Single Link transmission system

For the 8bit Single Link transmission system, 2 TMDS lines (for data) and 1 CLK line, a total of 3 differential signals will be used. The interleave mode switch should be set OFF during the data transmission. The Figure 2-1-2 shows the 8bit Single Link transmission system at resolution 1024 x 768, dot clock 75MHz.



ig. 2-1-4 8bit Single Link data transmission system

2.2. Layout of connector pin

2.2.1. DVI digital serial input connector

- Connector: DVI-I (74320-1004) made by Molex
- Input signal : TMDS

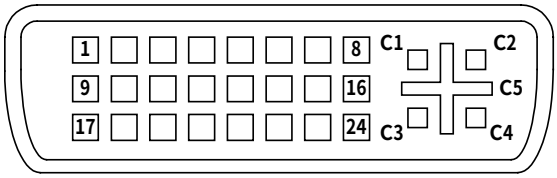


Fig. 2-2-1 Pin layout

Table 2-2-1 Pin numbers

Pin No	Signal	Pin No	Signal
1	TMDS DATA2−	16	SENSE
2	TMDS DATA2+	17	TMDS DATA0−
3	TMDS DATA2/4 G	18	TMDS DATA0+
4	TMDS DATA4−	19	TMDS DATA0-5 G
5	TMDS DATA4+	20	TMDS DATA5−
6	DDC CLK	21	TMDS DATA5+
7	DDC DATA	22	TMDS CLK G
8	—	23	TMDS CLK+
9	TMDS DATA1−	24	TMDS CLK−
10	TMDS DATA1+	C1	—
11	TMDS DATA1/3 G	C2	—
12	TMDS DATA3−	C3	—
13	TMDS DATA3+	C4	—
14	+5V	C5	—
15	GND	—	—

* TMDS DATA 0 to 2 for LINK #0, TMDS DATA 3 to 5 for LINK #1

2.2.2. LVDS output connector

- Connector: 10226-1210-VE made by 3M
- Output signal: LVDS

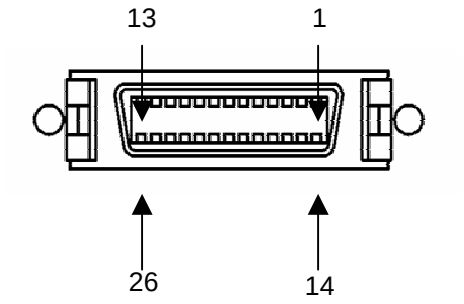


Fig. 2-2-2 Pin layout

Table 2-2-2 Pin numbers

LVDS 1CH

Pin.No	In/Out Signal	Pin.No	In/Out Signal	Pin.No	In/Out Signal
1	GND	10	TCLKG	19	TCG
2	TAG	11	+5V	20	TE-
3	SENS	12	TD-	21	TE+
4	TB-	13	TD+	22	TCLK-
5	TB+	14	TA-	23	TCLK+
6	TC-	15	TA+	24	NC
7	TC+	16	GND	25	TDG
8	TEG	17	TBG	26	GND
9	DDCSCL	18	DDCSDA	—	—

LVDS 2CH

Pin.No	In/Out Signal	Pin.No	In/Out Signal	Pin.No	In/Out Signal
1	GND	10	TCLKG	19	TCG
2	TAG	11	+5V	20	TE-
3	SENS	12	TD-	21	TE+
4	TB-	13	TD+	22	TCLK-
5	TB+	14	TA-	23	TCLK+
6	TC-	15	TA+	24	NC
7	TC+	16	GND	25	TDG
8	TEG	17	TBG	26	GND
9	DDCSCL	18	DDCSDA	—	—

2.3. Device input pin support

2.3.1. 12bit LVDS transmitter device pin support

- The table below shows the correspondence between the data output pins of the 12bit LVDS transmitter and the RGB data.
- The figure 2-3-1 shows the data transmission system
- LVDS transmitter: THC63LVD103 [THINE]

Table 2-3-1 12bit LVDS device pin support table

DVI pin assignment	LVDS pin assignment
R0 (LINK #1)	TB0 CH2)
R1 (LINK #1)	TB1 (CH2)
R2 (LINK #1)	TA0 (CH2)
R3 (LINK #1)	TA1 (CH2)
R0 (LINK #0)	TD0 (CH1)
R1 (LINK #0)	TD1 (CH1)
R2 (LINK #0)	TA0(CH1)
R3 (LINK #0)	TA1 (CH1)
R4 (LINK #0)	TA2 (CH1)
R5 (LINK #0)	TA3 (CH1)
R6 (LINK #0)	TA4 (CH1)
R7 (LINK #0)	TA5 (CH1)
G0 (LINK #1)	TB2 (CH2)
G1 (LINK #1)	TB3 (CH2)
G2 (LINK #1)	TA2 (CH2)
G3 (LINK #1)	TA3 (CH2)
G0 (LINK #0)	TD2 (CH1)
G1 (LINK #0)	TD3 (CH1)
G2 (LINK #0)	TA6 (CH1)
G3 (LINK #0)	TB0 (CH1)
G4 (LINK #0)	TB1 (CH1)
G5 (LINK #0)	TB2 (CH1)
G6 (LINK #0)	TB3 (CH1)
G7 (LINK #0)	TB4 (CH1)
B0 (LINK #1)	TB4 (CH2)
B1 (LINK #1)	TB5 (CH2)
B2 (LINK #1)	TA4 (CH2)
B3 (LINK #1)	TA5 (CH2)
B0 (LINK #0)	TD4 (CH1)
B1 (LINK #0)	TD5 (CH1)
B2 (LINK #0)	TB5 (CH1)
B3 (LINK #0)	TB6 (CH1)
B4 (LINK #0)	TC0 (CH1)
B5 (LINK #0)	TC1 (CH1)
B6 (LINK #0)	TC2 (CH1)
B7 (LINK #0)	TC3 (CH1)
HS (LINK #0)	TC4 (CH1)
VS (LINK #0)	TC5 (CH1)
DISP (LINK #0)	TC6 (CH1)

2.3.2. 10 bit LVDS transmitter device pin support

- The table below shows the correspondence between the data output pins of the 10bit LVDS transmitter and the RGB data.
- The figure 2-3-1 shows the data transmission system
- LVDS transmitter: THC63LVD103 [THINE]

Table 2-3-2 10bit LVDS device pin support table

DVI pin assignment	LVDS pin assignment
R0 (LINK #1)	TA0 (CH2)
R1 (LINK #1)	TA1 (CH2)
R0 (LINK #0)	TD0 (CH1)
R1 (LINK #0)	TD1 (CH1)
R2 (LINK #0)	TA0 (CH1)
R3 (LINK #0)	TA1 (CH1)
R4 (LINK #0)	TA2 (CH1)
R5 (LINK #0)	TA3 (CH1)
R6 (LINK #0)	TA4 (CH1)
R7 (LINK #0)	TA5 (CH1)
G0 (LINK #1)	TA2 (CH2)
G1 (LINK #1)	TA3 (CH2)
G0 (LINK #0)	TD2 (CH1)
G1 (LINK #0)	TD3 (CH1)
G2 (LINK #0)	TA6 (CH1)
G3 (LINK #0)	TB0 (CH1)
G4 (LINK #0)	TB1 (CH1)
G5 (LINK #0)	TB2 (CH1)
G6 (LINK #0)	TB3 (CH1)
G7 (LINK #0)	TB4 (CH1)
B0 (LINK #1)	TA4 (CH2)
B1 (LINK #1)	TA5 (CH2)
B0 (LINK #0)	TD4 (CH1)
B1 (LINK #0)	TD5 (CH1)
B2 (LINK #0)	TB5 (CH1)
B3 (LINK #0)	TB6 (CH1)
B4 (LINK #0)	TC0 (CH1)
B5 (LINK #0)	TC1 (CH1)
B6 (LINK #0)	TC2 (CH1)
B7 (LINK #0)	TC3 (CH1)
HS (LINK #0)	TC4 (CH1)
VS (LINK #0)	TC5 (CH1)
DISP (LINK #0)	TC6 (CH1)

2.3.3. 8 bit LVDS transmitter device pin support

- The table below shows the correspondence between the data output pins of the 8bit LVDS transmitter and the RGB data.
- The figure 2-3-1 shows the data transmission system
- LVDS transmitter: THC63LVD103 [THINE]

Table 2-3-3 8bit LVDS device pin support table

DVI pin assignment	LVDS pin assignment
R0 (LINK #0)	TD0 (CH1)
R1 (LINK #0)	TD1 (CH1)
R2 (LINK #0)	TA0 (CH1)
R3 (LINK #0)	TA1 (CH1)
R4 (LINK #0)	TA2 (CH1)
R5 (LINK #0)	TA3 (CH1)
R6 (LINK #0)	TA4 (CH1)
R7 (LINK #0)	TA5 (CH1)
G0 (LINK #0)	TD2 (CH1)
G1 (LINK #0)	TD3 (CH1)
G2 (LINK #0)	TA6 (CH1)
G3 (LINK #0)	TB0 (CH1)
G4 (LINK #0)	TB1 (CH1)
G5 (LINK #0)	TB2 (CH1)
G6 (LINK #0)	TB3 (CH1)
G7 (LINK #0)	TB4 (CH1)
B0 (LINK #0)	TD4 (CH1)
B1 (LINK #0)	TD5 (CH1)
B2 (LINK #0)	TB5 (CH1)
B3 (LINK #0)	TB6 (CH1)
B4 (LINK #0)	TC0 (CH1)
B5 (LINK #0)	TC1 (CH1)
B6 (LINK #0)	TC2 (CH1)
B7 (LINK #0)	TC3 (CH1)
HS (LINK #0)	TC4 (CH1)
VS (LINK #0)	TC5 (CH1)
DISP (LINK #0)	TC6 (CH1)

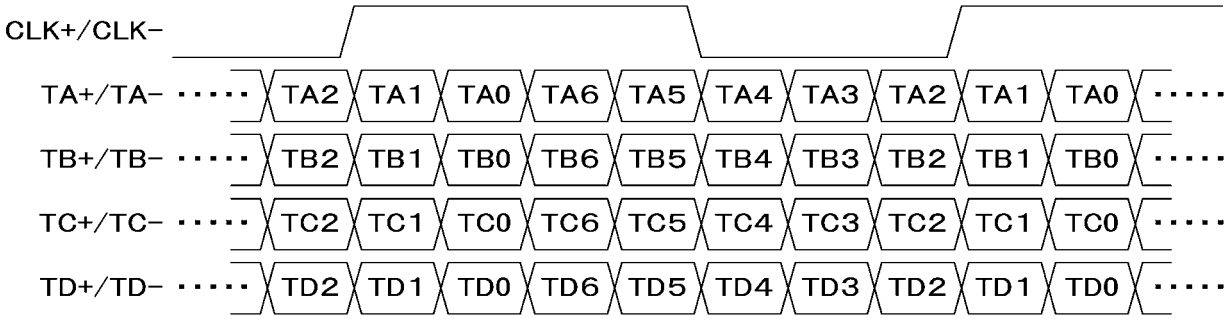

CLK+/CLK−
TA+/TA− ····· TA2 TA1 TA0 TA6 TA5 TA4 TA3 TA2 TA1 TA0 ·····
TB+/TB− ····· TB2 TB1 TB0 TB6 TB5 TB4 TB3 TB2 TB1 TB0 ·····
TC+/TC− ····· TC2 TC1 TC0 TC6 TC5 TC4 TC3 TC2 TC1 TC0 ·····
TD+/TD− ····· TD2 TD1 TD0 TD6 TD5 TD4 TD3 TD2 TD1 TD0 ·····

Fig. 2-3-2 Data transmission system

2.4. IA-573-A specifications

2.4.1. Specifications

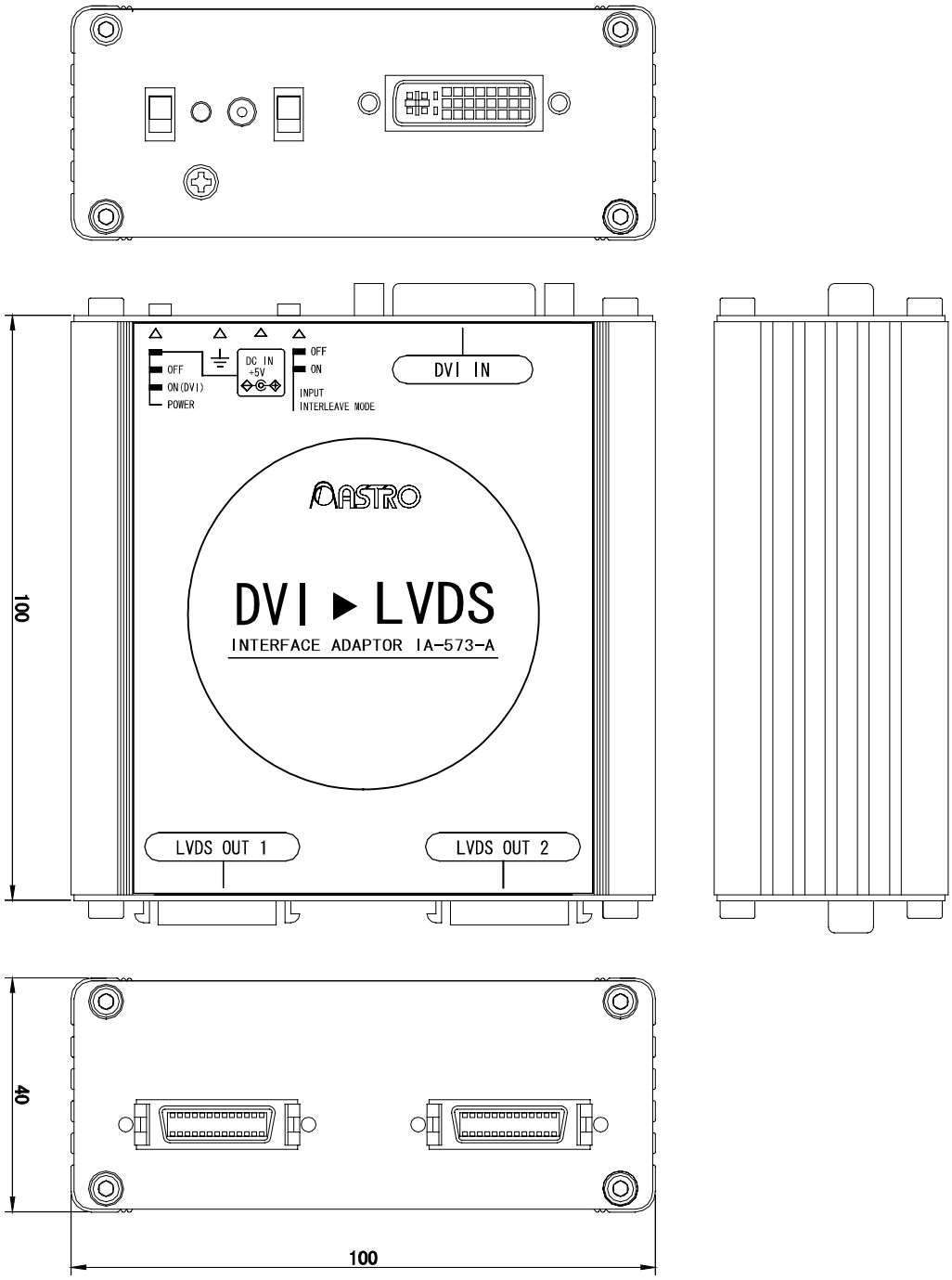
Dot clock frequency	8bit	SINGLE LINK	25 to 135MHz
	10bit	Interleave mode ON	12.5 to 82.5 (Transmission rate: 25 to 135MHz)
		Interleave mode OFF	25 to 135MHz
DVI Input			Compliant with DVI 1.0
LVDS Output			Compliant with DISM 1.0

*1: Use of the 2-meter cable made by Molex is recommended as the DVI cable.

2.4.2. Ratings

Supply voltage	DC5V
Power consumption	3.5W MAX
Dimensions	100(W)×100(H)×40(D)mm (excluding projections)
Weight	Approx. 0.5 kg
Operating temperature	5 to 40°C
Storage temperature	-10 to 60°C
Humidity	30 to 85%RH (no condensation)

2.4.3. Dimensional outline drawing



IA-573-A User's Manual

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- This manual may not be copied in whole or in part without written permission.
- The contents of this manual are subject to change without prior notice due to improvements.
- The manufacturer will not be liable for any effects caused by incorrect operation.
- All inquiries concerning this product should be addressed to your dealer or to the manufacturer at the contact numbers given below.
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T0078A

ASTRODESIGN,Inc.
URL http://www.astrodesign.co.jp
Sales and Marketing Devision
TEL: +81 3-5720-5300 FAX: +81 3-5720-6353
2-6-17, Haramachi, Meguro-ku, Tokyo 152-0011 Japan